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| 10/016,693 | 10/30/2001 | Michael D. Lammert | 12-1233 | 2474 |

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PATENT ADMINISTRATOR
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| EXAMINER | |
|---|---|
| MALDONADO, JULIO J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2823 | |

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/016,693 | LAMMERT, MICHAEL D. | |
| | Examiner | Art Unit | |
| | Julio J. Maldonado | 2823 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *13-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brighton et al. (U.S. 5,132,775) in view of Rhodes et al. (U.S. 4,536,951) and Wolf (Silicon Processing for the VLSI Era, Volume 2: Process Integration).

Brighton et al. (Figs.1-6) teach a method of forming interconnects including providing a semiconductor device (10) having a lower level layer including insulation layers (column 5, lines 3 – 10); forming a seed layer (22) on top of said lower level layer; forming a lower metal layer (12) on said seed layer (22); forming one pair of spaced apart vias (28) from a photoresist (26) on said lower metal layer (12); plating said spaced apart vias (28) defining plated pillars (16); removing the seed layer (22) not under the lower metal layer (12); forming on said one or more plated pillars and said seed layer with a dielectric layer (42) which can be planarized to expose said top surfaces of said plated pillars (column 4, lines 46 – 68); and forming a metal layer (44) to contact said exposed top surfaces of said plated pillars (16) (column 2, line 66 – column 6, line 19).

Brighton et al. fail to teach wherein said dielectric material is a low dielectric polymer coated and cured on said one or more plated pillars and seed layer. However,

Rhodes et al. (Figs.1-5) teach a method of forming a layered structure including the steps of forming a lower metal layer (2) on a surface of a substrate (4); forming an upper metal layer (8) on said lower metal layer (2); and forming on said lower metal layer (2) and said upper metal layer (8) a polyimide layer (12), wherein said forming further includes coating and curing said polyimide (12), wherein the metal layers are selected from the group including aluminum and copper (column 2, line 61 – column 3, line 50).

Furthermore, according to Wolf (Silicon Processing for the VLSI Era, Volume 2: Process Integration, pages 214 and 215) polyimides are well-known material used as planarizing interlevel dielectric layers because it can tolerate high temperatures without degradation, low dielectric constant and are free of pinholes and cracks.

Therefore, It would have been within the scope of one of ordinary skill in the art to combine the teachings of Brighton et al. and Rhodes et al. to enable forming the dielectric layer in Brighton et al. according to the teachings of Rhodes because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the dielectric layer of Brighton et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

3. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brighton et al. (U.S. 5,132,775) in view of Rhodes et al. (U.S. 4,536,951), Wolf (Silicon Processing for the VLSI Era, Volume 2: Process Integration) and Lee et al. (U.S. 6,800,928 B1).

Brighton et al. (Figs.1-6) teach a method of forming interconnects including providing a semiconductor device (10) having a lower level layer including insulation layers (column 5, lines 3 – 10); forming a seed layer (22) on top of said lower level layer; forming a lower metal layer (12) on said seed layer (22); forming one pair of spaced apart vias (28) from a photoresist (26) on said lower metal layer (12); plating said spaced apart vias (28) defining plated pillars (16); removing the seed layer (22) not under the lower metal layer (12); forming on said one or more plated pillars and said seed layer with a dielectric layer (42) which can be planarized to expose said top surfaces of said plated pillars (16 and column 4, lines 46 – 68); and forming a metal layer (44) to contact said exposed top surfaces of said plated pillars (16) (column 2, line 66 – column 6, line 19).

Brighton et al. fail to teach wherein said dielectric material is a low dielectric polymer coated and cured on said one or more plated pillars and seed layer. However, Rhodes et al. (Figs.1-5) teach a method of forming a layered structure including the steps of forming a lower metal layer (2) on a surface of a substrate (4); forming an upper metal layer (8) on said lower metal layer (2); and forming on said lower metal layer (2) and said upper metal layer (8) a polyimide layer (12), wherein said forming further includes coating and curing said polyimide (12), wherein the metal layers are selected from the group including aluminum and copper (column 2, line 61 – column 3, line 50).

Furthermore, according to Wolf (Silicon Processing for the VLSI Era, Volume 2: Process Integration, pages 214 and 215) polyimides are well-known material used as

planarizing interlevel dielectric layers because it can tolerate high temperatures without degradation, low dielectric constant and are free of pinholes and cracks.

Therefore, It would have been within the scope of one of ordinary skill in the art to combine the teachings of Brighton et al. and Rhodes et al. to enable forming the dielectric layer in Brighton et al. according to the teachings of Rhodes because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the dielectric layer of Brighton et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combined teachings of Brighton et al., Rhodes et al. and Wolf fail to teach wherein said coating step comprises coating with a low dielectric, non-planarizing polymer and forming a planarizing coating over said non-planarizing polymer. However, Lee et al. (Figs.1F and 2A) teach a method of forming a low-dielectric coating on a series of metal pillars (130), wherein in one embodiment of the invention includes coating with a low dielectric polymer (142) that can be planarized, and in a second embodiment of the invention includes coating with a low dielectric, non-planarizing polymer (242) and forming a planarizing coating (244) over said non-planarizing polymer (242) (column 4, line 63 – column 5, line 51).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Brighton et al., Rhodes et al. and Wolf with Lee et al. to enable the coating step of Brighton et al., Rhodes et al. and Wolf to be performed according to the teachings of Lee et al. because one of ordinary skill in the art at the time the

invention was made would have been motivated to look to alternative suitable methods of performing the disclosed coating step of Brighton et al., Rhodes et al. and Wolf and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

4. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brighton et al. (U.S. 5,132,775) in view of Rhodes et al. (U.S. 4,536,951) and Wolf (Silicon Processing for the VLSI Era, Volume 2: Process Integration) as applied to claims 1 and 2 above, and further in view of Lin (U.S. 5,929,525).

The combined teachings of Brighton et al., Rhodes et al. and Wolf substantially teach all aspects of the invention but fail to disclose applying a dielectric layer over the lower and upper metal layer before said low dielectric polymer coating is applied, wherein said dielectric layer is selected from the group including silicon oxide. However, Lin (Figs.1-9) teach a method of forming multilevel interconnects including the steps of providing a metal pillar (12) on a lower metal layer (9); and applying a silicon oxide layer (13) on the lower metal layer (9) and the metal pillar (12) (column 4, lines 19 – 44). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention made to enable forming the dielectric layer disclosed in Lin in the multilevel interconnect method of Brighton et al., Rhodes et al. and Wolf because this would provide passivation for the metal pillar structures (column 4, lines 19 – 44).

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brighton et al. (U.S. 5,132,775) in view of Rhodes et al. (U.S. 4,536,951), Wolf (Silicon Processing for the VLSI Era, Volume 2: Process Integration) and Lin (U.S. 5,929,525)

as applied to claims 1, 2, 4 and 5 above, and further in view of Tsai et al. (U.S. 5,252,515).

The combination of Brighton et al., Rhodes et al., Wolf and Lin teach applying a dielectric layer comprising silicon oxide (Lin, column 4, lines 19 – 44), but fail to teach the dielectric layer comprising silicon nitride. However, Tsai et al. teach a method of forming an interconnect structure including the steps of forming a passivation layer (23); and coating said passivation layer (22, 23) with an SOG layer (24), wherein said passivation layer (23) is either silicon oxide or silicon nitride (Tsai et al., column 5, lines 1 – 49). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Brighton et al., Rhodes et al., Wolf and Lin with Tsai et al. to enable forming the passivation layer of Brighton et al., Rhodes et al., Wolf and Lin using the materials according to the teachings of Tsai et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed passivation layer of Brighton et al., Rhodes et al., Wolf and Lin and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

6. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brighton et al. (U.S. 5,132,775) in view of Rhodes et al. (U.S. 4,536,951) and Wolf (Silicon Processing for the VLSI Era, Volume 2: Process Integration) as applied to claims 1 and 2 above, and further in view of Hendricks et al. (U.S. 6,153,525).

The combined teachings of Brighton et al., Rhodes et al. and Wolf substantially teach all aspects of the invention but fail to disclose wherein the step of coating

comprises coating said one or more plated pillars and said lower metal layer with a silicon-based polymer. However, Hendricks et al. teach a method of forming a planarized dielectric layer by spin-on techniques, wherein said layer is selected from the group including polyimides, silicon-based polymers and benzocyclobutene (column 4, lines 13 – 20). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Brighton et al., Rhodes et al. and Wolf with Hendricks et al. to enable forming the dielectric layer of Brighton et al., Rhodes et al. and Wolf according to the teachings of Hendricks et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed dielectric layer of Brighton et al., Rhodes et al. and Wolf and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brighton et al. (U.S. 5,132,775) in view of Rhodes et al. (U.S. 4,536,951), Wolf (Silicon Processing for the VLSI Era, Volume 2: Process Integration) and Hendricks et al. (U.S. 6,153,525) as applied to claims 1, 2, 7 and 8 above, and further in view of the Applicants' Admitted Prior Art.

The combined teachings of Brighton et al., Rhodes et al., Wolf and Hendricks et al. substantially teach all aspects of the invention but fail to disclose coating the lower metal layer and the plated pillars with polynorbornene. However, the submitted prior art teaches wherein in practical applications, a polymer such as benzocyclobutene and polynorbornene, is known to be coated over a conventional dielectric, such as silicon

dioxide or silicon nitride, on a wafer with metal layers and other topology formed thereon (page 1, [0003] – page 3, [0008]). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Brighton et al., Rhodes et al., Wolf and Hendricks et al. with the prior art to enable the applying and coating step of Brighton et al., Rhodes et al., Wolf and Hendricks et al. to be performed according to the teachings of the prior art because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed coating step of Brighton et al., Rhodes et al. and Wolf and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

8. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brighton et al. (U.S. 5,132,775) in view of Rhodes et al. (U.S. 4,536,951) and Wolf (Silicon Processing for the VLSI Era, Volume 2: Process Integration) as applied to claims 1 and 2 above, and further in view of Furukawa et al. (U.S. 6,387,783 B1).

The combined method of Brighton et al., Rhodes et al. and Wolf teach using a photoresist to form the plated pillars but fail to expressly teach using a photoresist with a re-entrant profile and using a negative i-line resist. However, Furukawa et al. (Figs.2A-2E) in a related method to pattern a metal layer teach using a photoresist (201) with a re-entrant profile and using a negative i-line resist (column 1, line 43 – 65). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Brighton et al., Rhodes et al. and Wolf with Furukawa et al. to enable using a photoresist as taught by Furukawa et al., since this

would improve linewidth control in a multilayered stack (Furukawa et al., column 1, lines 25 – 33).

9. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brighton et al. (U.S. 5,132,775) in view of Rhodes et al. (U.S. 4,536,951), Wolf (Silicon Processing for the VLSI Era, Volume 2: Process Integration) and Furukawa et al. (U.S. 6,387,783 B1) as applied to claims 1, 2, 10 and 11 above, and further in view of Samoto (U.S. 5,583,063).

The combined teachings of Brighton et al., Rhodes et al., Wolf and Furukawa et al. teach using a negative photoresist to define a pattern (Furukawa et al., column 1, line 43 – 65) but fail to expressly teach using a $NH_3$ image reversal of a photoresist. However, Samoto (Figs.2A-2H) in a related to define a pattern for a semiconductor device teaches using a $NH_3$ image reversal of a photoresist (column 4, lines 18 – 36). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the photoresist of Samoto in the interconnect formation method of Brighton et al., Rhodes et al., Wolf and Furukawa et al., since this would allow the formation of defined small-sized patterns (column 2, lines 47-50).

***Response to Arguments***

10. Applicant's arguments filed 04/24/2006 have been fully considered but they are not persuasive.

Applicants argue, "...none of the references recited plated photoresist pillars...". In response to applicants arguments, the recitation in claim 1, "...plating said pillars defining at least one pair of plated pillars having top surfaces...", is read as said pillars

being exposed to a plating process to form plated pillars. Furthermore, the disclosed specification teaches, "...Referring to FIG. 2, after the lower metal layer 26 is formed, any conventional photoresist 28, compatible with metal plating processes, is spun over the patterned bottom metal layer 26 and the seed layer 24. The photoresist layer 28 may be patterned by conventional techniques, such as photolithography, to form the patterned vias 30 and 32, for example. The photoresist layer 28 may be coated directly over the lower layer metal 26 and its resist or the lower layer metal resist may be first stripped and then the next layer of resist coated over the seed layer 24 and the lower layer metal 26. The vias 30 and 32 are plated, as discussed above, to form plated pillars 34 and 36 to height of, for example, 1 micrometer to 10 micrometers or more, using the same seed layer 24 as was used to plate the lower metal layer 26. The photoresist layer 28 is then stripped by conventional techniques. The seed layer 24 that is not under the lower layer metal 26 is then removed by wet chemical etching, a dry etch process or a combination of both..." (Instant paragraph [0027]). From the submitted disclosure, the photoresist pillars are exposed to a plating process to form plated pillars in the vias. This is also taught in the Brighton (see, for example column 3, lines 49 – 58). The submitted disclosure does not teach forming plated photoresist pillars.

***Conclusion***

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (http://portal.uspto.gov/external/portal/pair) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
June 30, 2006

George Fourson
Primary Examiner